TOGETHER FOR RISC-V TECHNOLOGY
& APPLICATIONS

RISC-V Summit Europe 2024

TRISTAN: Free Access Training on EDA tooling for RISC-V

09:00-11:30, Friday, 28.06.2024, Munich

TRISTAN has received funding from Chips Joint Undertaking (CHIPS-JU) under grant agreement nr. 101095947.

CHIPS JU receives support from the European Union's Horizon Europe's research and innovation programme and Austria, Belgium, Bulgaria, Croatia, Cyprus, Czechia, Germany, Denmark, Estonia, Greece, Spain, Finland, France, Hungary, Ireland, Israel, Iceland, Italy, Lithuania, Luxembourg, Latvia, Malta, Netherlands, Norway, Poland, Portugal, Romania, Sweden, Slovenia, Slovakia, Turkey

RISC-V Summit Europe 2024

TRISTAN: Free Access Training on EDA tooling for RISC-V

09:00-11:30, Friday, 28.06.2024, Munich

09:00-09:15 **Welcome and Brief Introduction to the TRISTAN EDA Tooling Landscape**
Bernhard Fischer (Siemens)

09:15-09:45 **Virtual Platform Modeling for RISC-V Systems**
Rocco Jonak (MINRES)

09:45-10:45 **CVE2 Industrial Verification**
Florian Wohlrab, Davide Schiavone, Mario Rodriguez (OpenHW Group)

10:45-11:15 **Experiences on IP Design with Open-Source and Commercial Tools**
Sara Bocchio (STMicroelectronics)

TOGETHER FOR RISC-V TECHNOLOGY
& APPLICATIONS

TRISTAN
RISC-V


TOGETHER FOR
RISC-V TECHNOLOGY
& APPLICATIONS
TRISTAN
RISC-V

EDA Tools are a significant part of the overarching goals of TRISTAN

https://tristan-project.eu

Expand, Mature, Industrialize the European RISC-V ecosystem to compete with existing commercial / proprietary alternatives

- Leveraging the Open-Source community to gain in productivity and quality
- Defining a European strategy for RISC-V based designs including the creation of a repository of industrial quality building blocks to be used for SoC designs in different application domains
- Applying a holistic approach, covering both electronic design automation tools (EDA) and the full software stack
- Exposing a large number of engineers to RISC-V technology, which will further strengthen adoption.

TRISTAN Consortium

46 Partners

€54m Budget

12/2022 Start date

NXP Lead

TRISTAN has received funding from Chips Joint Undertaking (CHIPS-JU) under grant agreement nr. 101095947.

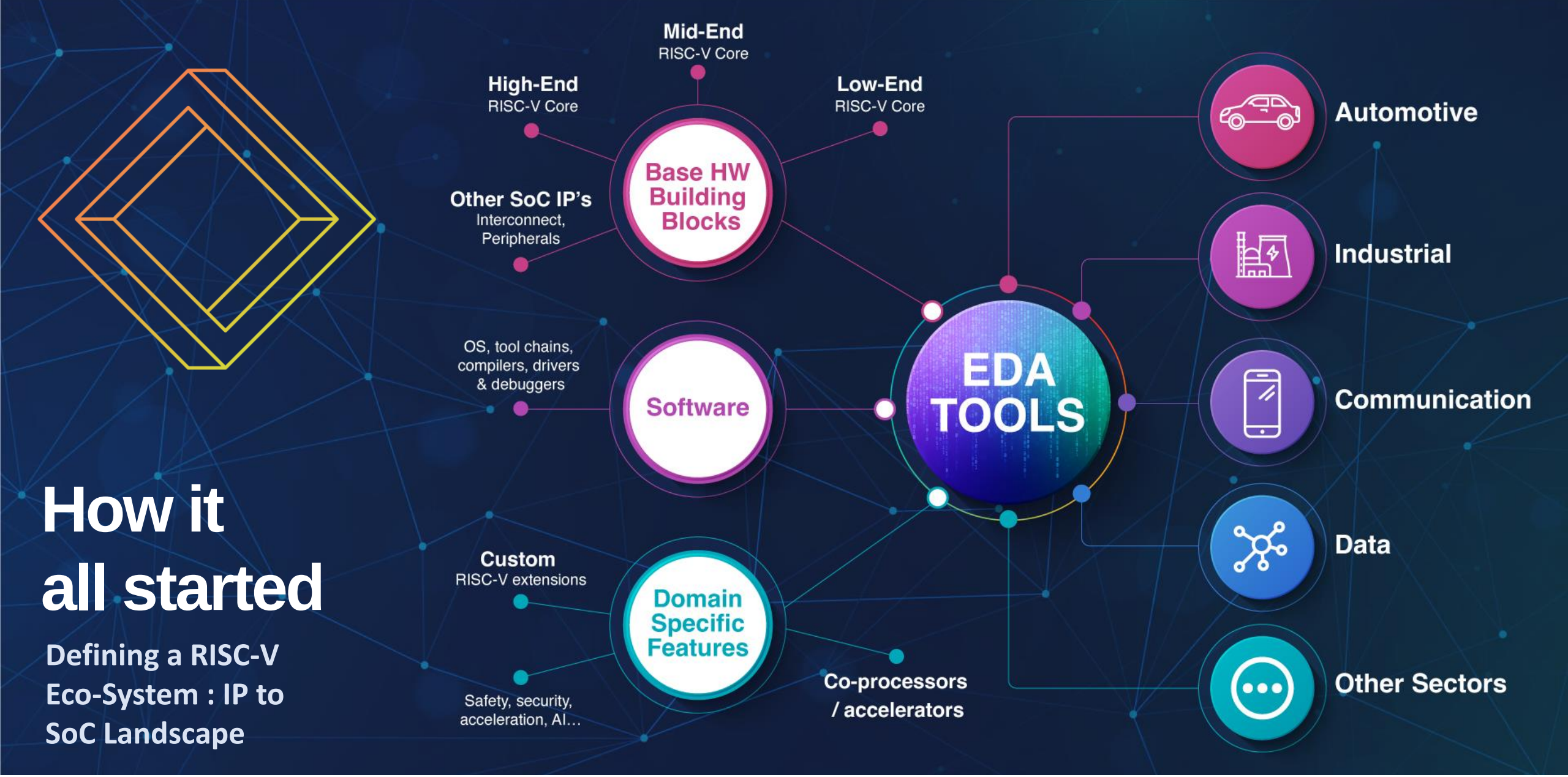
CHIPS JU receives support from the European Union's Horizon Europe's research and innovation programme and Austria, Belgium, Bulgaria, Croatia, Cyprus, Czechia, Germany, Denmark, Estonia, Greece, Spain, Finland, France, Hungary, Ireland, Israel, Iceland, Italy, Lithuania, Luxembourg, Latvia, Malta, Netherlands, Norway, Poland, Portugal, Romania, Sweden, Slovenia, Slovakia, Turkey

TRISTAN Consortium

Synergise, Complement and Build a strong European Network

TRISTAN has received funding from Chips Joint Undertaking (CHIPS-JU) under grant agreement nr. 101095947.

CHIPS JU receives support from the European Union's Horizon Europe's research and innovation programme and Austria, Belgium, Bulgaria, Croatia, Cyprus, Czechia, Germany, Denmark, Estonia, Greece, Spain, Finland, France, Hungary, Ireland, Israel, Iceland, Italy, Lithuania, Luxembourg, Latvia, Malta, Netherlands, Norway, Poland, Portugal, Romania, Sweden, Slovenia, Slovakia, Turkey



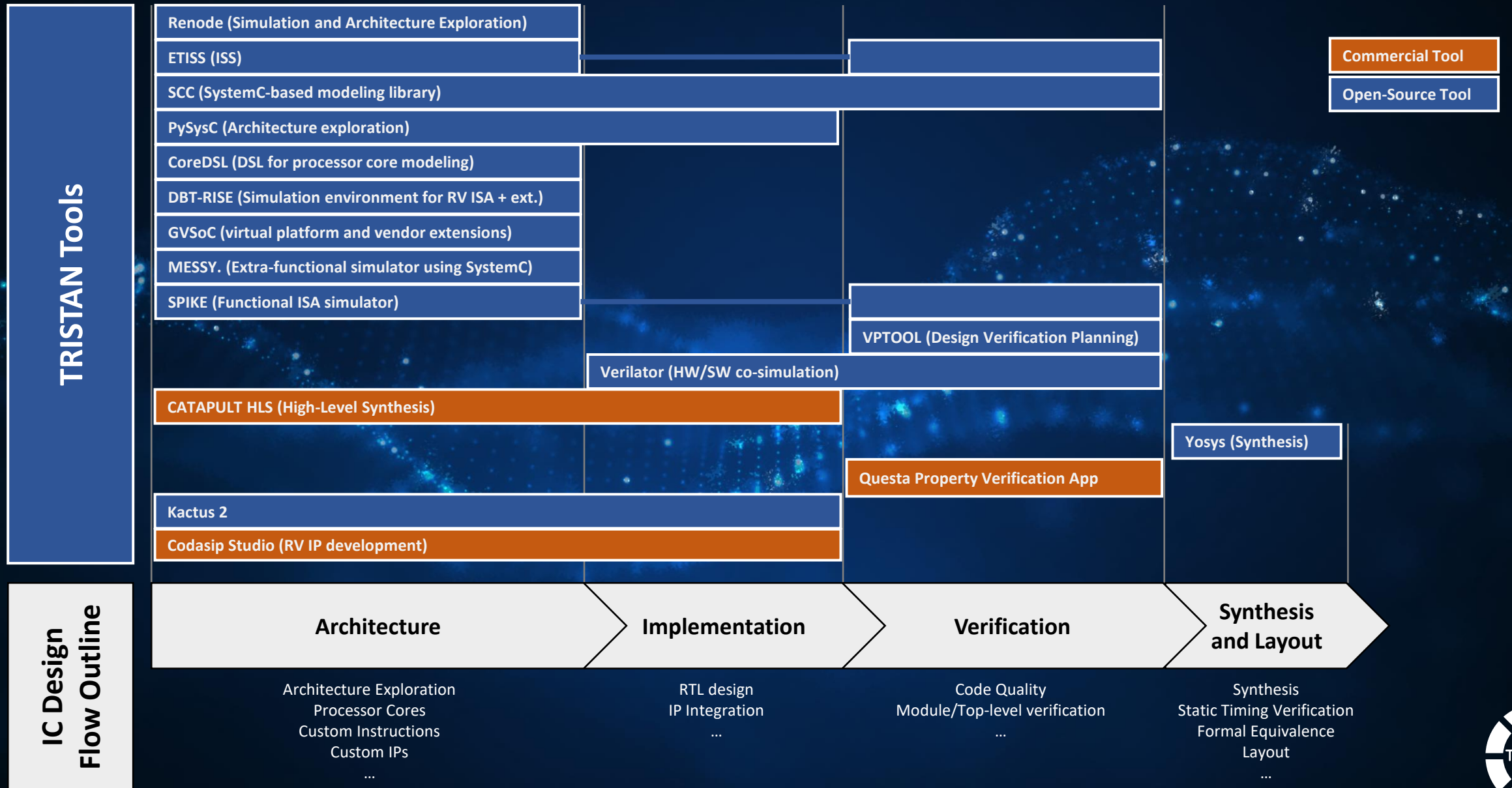
How it all started

Defining a RISC-V Eco-System : IP to SoC Landscape

TRISTAN has received funding from Chips Joint Undertaking (CHIPS-JU) under grant agreement nr. 101095947.

CHIPS JU receives support from the European Union's Horizon Europe's research and innovation programme and Austria, Belgium, Bulgaria, Croatia, Cyprus, Czechia, Germany, Denmark, Estonia, Greece, Spain, Finland, France, Hungary, Ireland, Israel, Iceland, Italy, Lithuania, Luxembourg, Latvia, Malta, Netherlands, Norway, Poland, Portugal, Romania, Sweden, Slovenia, Slovakia, Turkey

The TRISTAN EDA Tool Landscape



TRISTAN IP/Tools can be accessed through the Unified Access Page

TOOLS

Tool	URL/Instructions	TRISTAN Working Items	Owner/Contributors	Users	Description
Renode	Renode	WI5.1.1	Antmicro	Tampere University, NOKIA, Cargotec	Simulation Framework
ETISS	ETISS	WI5.1.2	Technische Universität München	Infineon	Extendible Translating Instruction Set Simulator
SCC	SCC	WI5.1.4	Minres	Bosch-DE, CEA	SystemC Components
PySysC	PySysC	WI5.1.4	Minres	Bosch-DE, CEA	Python bindings for SystemC
Core DSL	Core DSL	WI5.1.4	Minres	Bosch-DE, CEA	Language to describe ISAs for ISS generation and HLS of RTL implementation

TRISTAN IP/Tools can be accessed through the Unified Access Page

CORES

Repository	URL/Instructions	TRISTAN Working Items	Partners	Status
CVE2	CVE2	WI2.2.5, WI2.2.8, WI2.5.8	NXP, Synthara, Politecnico di Torino	Design and Verification in progress
Extensions to the micro-architecture of CV32E40P core	CV32E40P (fork)	WI2.3.3	UNIBO	Design and Verification in progress
VSRV1: simple 32-bit Linux RISC-V	To Be Done	WI2.3.5	VLSI Solution	Design and Verification in progress
CVA6	CVA6	WI2.4.1, WI2.4.2, WI2.4.3, WI2.4.5	Thales, Sysgo, TU Darmstadt, Bosch	Design and Verification in progress

TRISTAN IP/Tools can be accessed through the Unified Access Page

PERIPHERALS

Repository	URL/Instructions	TRISTAN Working Items	Partners
TSN-TraceBus	Not published yet	WI3.1.1	ACCT, BOSCH-DE, FHG, SYSGO
HPDcache	github.com/openhwgroup/cv-hpdcache	WI3.1.5	CEA
CLIC	clic	WI3.1.7	ETH

SOFTWARE

Repository	URL/Instructions	TRISTAN Working Items	Partners
TimeWeaver	absint.com/timeweaver	WI4.1.5	AbsInt
CompCert	github.com/AbsInt/CompCert	WI4.2.4	AbsInt
Yocto for CVA6	meta-cva6-yocto	WI4.3.3	Thales

TRISTAN
RISC-V

TOGETHER FOR
RISC-V TECHNOLOGY
& APPLICATIONS

TRISTAN webpage

TRISTAN LinkedIn

TRISTAN Unified Access Page

TRISTAN has received funding from Chips Joint Undertaking (CHIPS-JU) under grant agreement nr. 101095947.

CHIPS JU receives support from the European Union's Horizon Europe's research and innovation programme and Austria, Belgium, Bulgaria, Croatia, Cyprus, Czechia, Germany, Denmark, Estonia, Greece, Spain, Finland, France, Hungary, Ireland, Israel, Iceland, Italy, Lithuania, Luxembourg, Latvia, Malta, Netherlands, Norway, Poland, Portugal, Romania, Sweden, Slovenia, Slovakia, Turkey