Using a Performance Model to Implement a Superscalar CVA6

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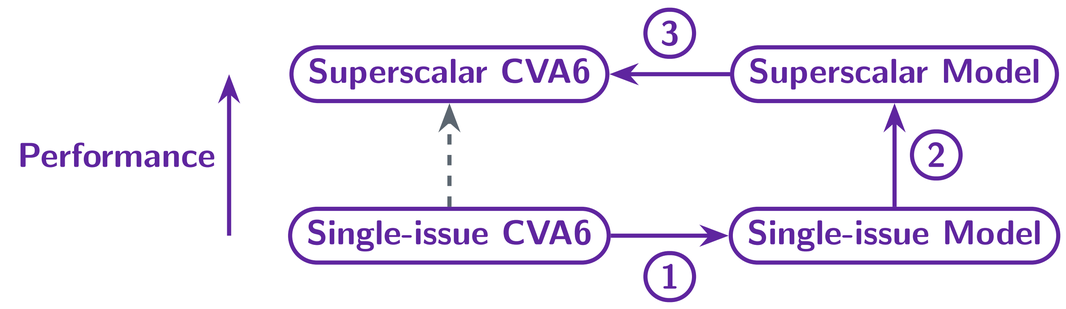
Context

- CVA6: a 32- or 64-bit RISC-V application processor
- Highly-configurable, 6-stage pipeline
- In-order issue, out-of-order execution
- Performance is **3.10 CoreMark/MHz** on single-issue

How to improve performance further?

Methodology



1. Cycle-Based Model

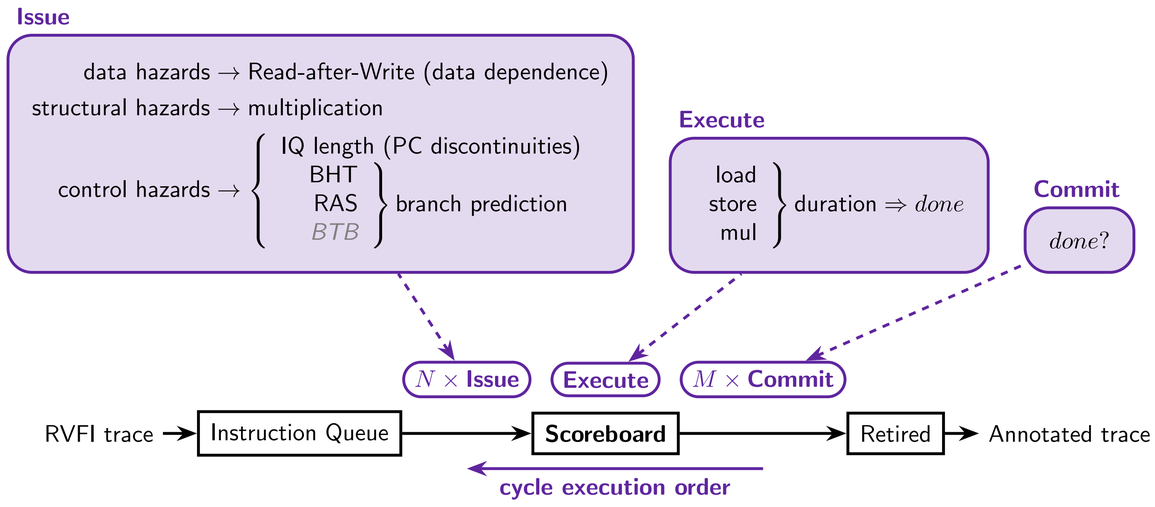
- **Goal** Easily evaluate architecture improvements
- **Input** RVFI trace (committed instr.s) from CVA6
- **Output** Cycle-annotated RVFI trace

Accuracy check:

- Using 2nd iteration of CoreMark
- Measure each instruction duration $\Delta t_i = t_i - t_{i-1}$
- Count correct results $\#\{i \mid \Delta t_i^{\text{Model}} = \Delta t_i^{\text{RTL}}\}$
- Divide by instruction number $\#\{i\}$

$$\text{Accuracy} = \frac{\#\{i \mid \Delta t_i^{\text{Model}} = \Delta t_i^{\text{RTL}}\}}{\#\{i\}} = \mathbf{99.2\,\%}$$

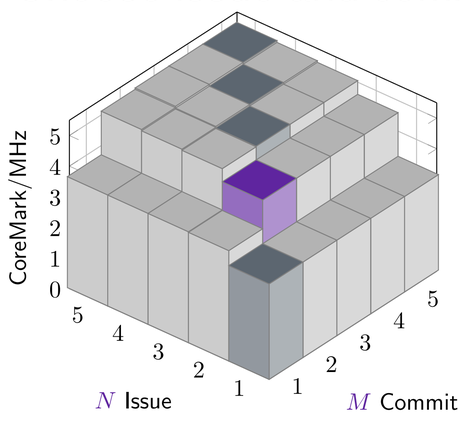
- **Issue** Check for interactions between instructions
- **Execute** Mark as done, delay according to instruction
- **Commit** Check for done mark



2. Predicting Performance

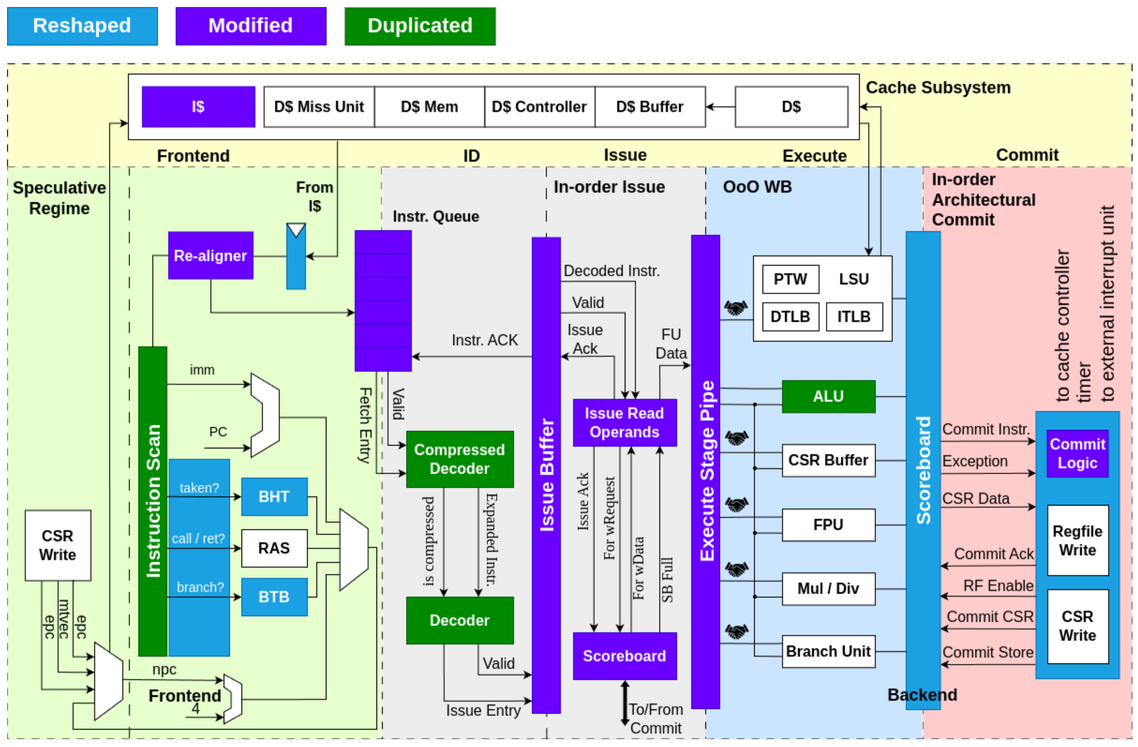
a. Add the feature in the Python `Model` class: the **data path is ignored** here
b. For a given benchmark, the model produces the performance gain considering the whole pipeline even though the modification (a.) was local
c. **Implement**, **rework** or **discard** the feature

- **Superscalar** Choose issue and commit port numbers



- **Dual-issue** Final prediction for **performance gain**
  - With renaming: **+47% speed**
  - Without renaming: **+42% speed**

3. Implementing Superscalar CVA6



Debug the performance by comparing with the model:

- (α) **Global performance** Performance gain
- (β) **Local performance** Instructions duration
- (γ) **Internal** Pipeline state over time

Results

Criteria	Reference	Superscalar	Variation
CoreMark/MHz	**3.10**	**4.35**	**+40.1%**
Max. Frequency	892 MHz	877 MHz	-1.75%
Power	32.453 mW	34.844 mW	+7.37%
Area	250 kGE	278 kGE	+11.1%

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